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# ENHANCING VERTICAL $GA_2O_3$ POWER DEVICES VIA CURRENT BLOCKING LAYER INNOVATION

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***Abstract:*** *Beta-gallium oxide ($\beta$-$Ga_2O_3$) has emerged as a compelling material for next-generation power electronics, owing to its ultra-wide bandgap of 4.8 eV and high critical electric field of 8 MV/cm. These properties, along with the availability of melt-grown substrates, position $\beta$-$Ga_2O_3$ as a key contender for high-voltage device applications. However, the lack of effective p-type doping—due to highly localized holes and large acceptor activation energies—presents a major challenge to implementing traditional n–p–n vertical power transistors. To address this limitation, recent research has focused on the integration of a current-blocking layer (CBL), which can replicate the role of a p-type region in vertical device architectures. This perspective reviews the progress in CBL-based designs within vertical $\beta$-$Ga_2O_3$ MOSFETs and highlights emerging concepts such as the Mg-diffused CBL for enabling vertical diffused barrier field-effect transistors (VDBFETs). The potential of CBL technology to overcome the doping bottleneck and enable scalable, high-performance vertical devices is discussed.*

***Keywords:*** *$\beta$-$Ga_2O_3$ MOSFETs, current-blocking layer, vertical power devices, wide bandgap semiconductors*

## 1. Introduction

The rapid electrification of energy sources in every sector of our lives (figure 1(a)), such as in electric cars (EVs) and solar/wind power farms, calls for an increasingly efficient and more compact power conversion technology. Modern power converters use numerous semiconductor switches to modulate the form of electric power, for example, from DC to AC in the traction inverters of the EV drivetrain. These semiconductor switches are traditionally made with silicon. However, by replacing silicon with materials with a larger bandgap shown in figure 1(b) that can handle higher power, the energy loss in the conversion stage can be drastically reduced while shrinking the converter system footprint. In particular, beta-gallium oxide ($\beta$-$Ga_2O_3$) can potentially provide even better performance compared to commercially used wide bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) at a fraction of the cost [1–4].

It ultra-WBG of 4.8 eV enables devices with exceptionally high breakdown voltages and the ability to operate at elevated temperatures, ideal for high-power applications. In addition, the large bandgap

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gives rise to a significantly higher unipolar power figure-of-merit (PFoM), suggesting great potential for higher power densities and efficiencies compared to current technologies.

Figure 1(b) showcases several commonly studied WBG materials in comparison with first-generation semiconductor Si and GaAs. Among all the wide-bandgap semiconductors, $\beta$-$Ga_2O_3$ is the only material with large diameter (>4″) wafers that can be grown via melt growth technology [5–7], which ensures both high material quality and low-cost production, making rapid commercialization of the technology feasible. As such, $\beta$-$Ga_2O_3$ power device research activity has undergone a significant surge in the past decade [8–13]. So far, substantial progress has been made toward high-voltage and high-performance $Ga_2O_3$ diodes and lateral FETs by utilizing different techniques to mitigate parasitic breakdown and tap into the ultimate potential of the 8 MV $cm^{-1}$ breakdown limit. Notably, multi-kV and ultra-high breakdown voltages of 8–10 kVs have been measured in lateral MESFETs and MOSFETs [10, 14–20]. Heterojunction diodes



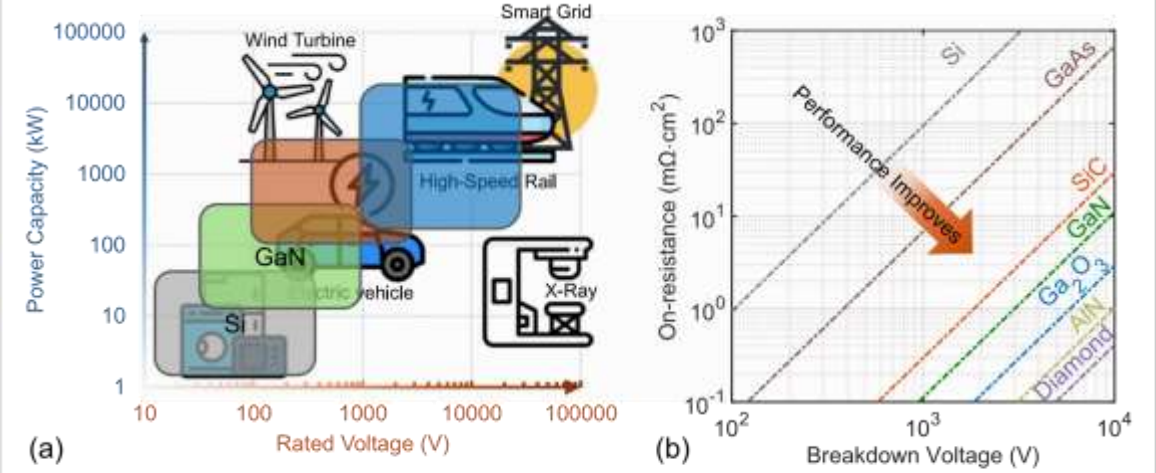


**Figure 1.** (a) The voltage and power ratings of different WBG semiconductor technologies overlaying on top of various application areas of interest. (b) Constant power figure of merit contour lines for several WBG materials. The bottom right corner is the desired performance location. The power figure of merit is calculated assuming the ideal bulk material properties.

[21–25], especially consisting of p-NiO/$\beta$-$Ga_2O_3$ layers have achieved a measured breakdown of >10 kV, an average electric field of 6.2 MV $cm^{-1}$, and a PFoM surpassing the theoretical limit of GaN and SiC [26–29]. These results indicate an immense potential of $\beta$-$Ga_2O_3$ to revolutionize high-power semiconductor device field. However, the PFoM of $\beta$-$Ga_2O_3$ vertical transistors continues to fall short of its SiC counterpart mainly due to the lack of effective p-type doping, which poses inherent challenges to the engineering of high-voltage $Ga_2O_3$ vertical devices. The extremely flat oxygen 2p orbit at the valence band maximum of $\beta$-$Ga_2O_3$ effectively traps any holes, forming a small polaron, resulting in a high hole effective mass [30, 31]. This makes uniform charge balancing in the vertical devices difficult, which is essential for p-body/gate layers, edge-termination, and super-junction structures.

Vertical power transistors are considered the holy grail of power semiconductor devices and are widely used in high-power applications, such as electric transportation. The state-of-the-art SiC MOSFETs are usually enhancement mode vertical devices with a U-shaped trench gate. These devices boast high

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blocking voltages (up to 1700 V), fast switching speeds, and reduced on-resistance compared to Si insulated-gate bipolar transistors (IGBT) but are only used in high-end EV applications due to cost. In lower-end EV models, Si IBGTs, also a vertical structure device, are still widely used. Compared to lateral devices shown in figure 2(a), vertical structures in figures 2(b) and (c) allow for a larger drift region expanding in the vertical direction without compromising chip surface area. This means it can support higher voltages, resulting in a higher power density. In addition, the vertical structure provides a larger cross-sectional area for current flow, leading to a reduced on-state resistance ($R_{ds(on)}$), contributing to a lower conduction loss during power switching operations. Vertical MOSFETs also offer better thermal management options, which is crucial for $Ga_2O_3$ electronics due to the relatively low thermal conductivity of the material. Within the vertical devices, heat is produced throughout their volume rather than just at the surface [32]. This configuration offers greater flexibility in developing thermal management solutions, such as heat sinks or cooling systems, which are essential for maintaining optimal operating temperatures and ensuring reliable performance.

Traditionally, vertical power Si and SiC transistors are implemented with an n–p–n junction consisting of a buried p-type layer, as shown in figure 3 [33, 34]. The design and implementation of this p-layer are crucial for achieving high voltage blocking and low on-resistance. However, unlike Si and SiC, effective p-type doping in $Ga_2O_3$ has not been demonstrated so far due to highly localized holes and a large acceptor activation energy, making high-performance vertical $Ga_2O_3$ transistors extremely challenging to realize. Several methods to circumvent this problem have been proposed, and corresponding devices were experimentally demonstrated- all with their advantages and drawbacks. On a high level, there are three types of solutions to tackle the lack of p-type doping: First, to etch the channel into a very thin vertical fin and pinch it off from both sides, as shown in figure 2(b), such transistors have the same structure as FinFETs used in state-of-art low power logic devices, thus are named the same [35]. Only in this case the FinFET structure is adopted and optimized for high-power applications; Second, to use another p-type material (such as
$NiO_x$) and integrate it heterogeneously into the $Ga_2O_3$ system forming a hetero-junction device [22, 26, 36, 37]; Third, to use a quasi p-layer (for example, with deep traps) to serve the same functionality as a conductive p-layer, as shown in figure 2(c) [38–43]. Although the realization of conductive p-type layers remains elusive, many dopants and processing treatments in $Ga_2O_3$ have resulted in highly resistive layers

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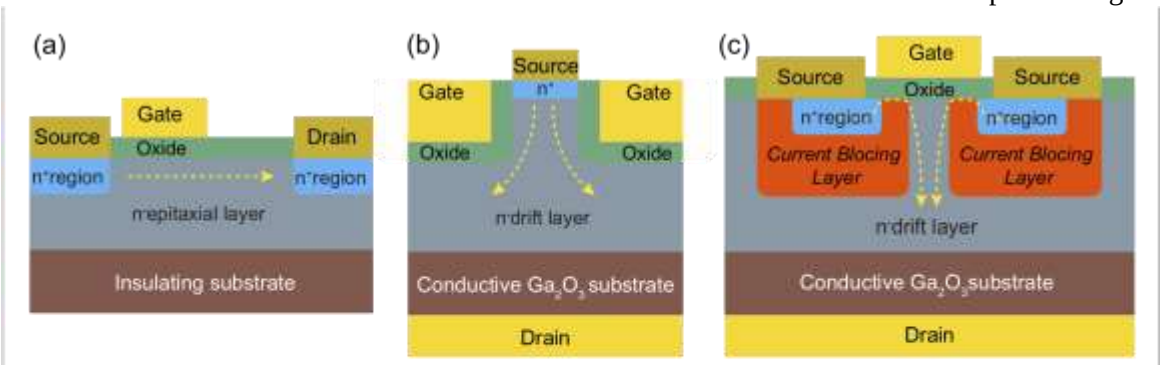


**Figure 2.** Cross-section schematics of $Ga_2O_3$ (a) lateral MOSFET, (b) vertical FinFET, and (c) vertical MOSFET with current blocking layer. Each structure is a general representation of different variations of the similar kind. Yellow dashed lines indicate the flow of electrons in the channel during on-state.

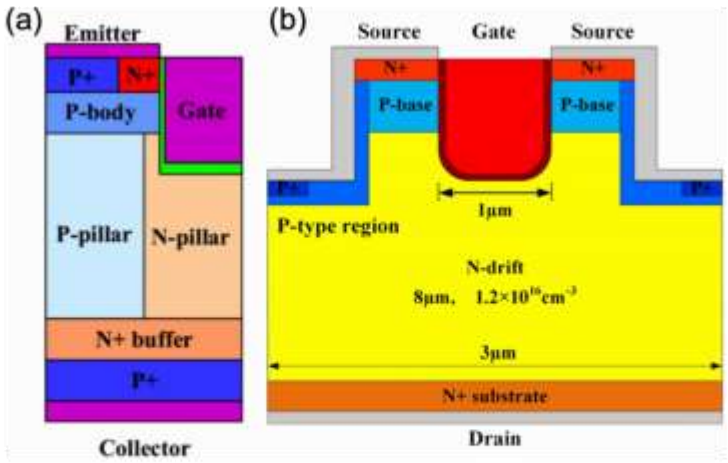


**Figure 3.** Representative structures of commercially available (a) superjunction type Si IGBT. © 2020 IEEE. Reprinted, with permission, from [33]. (b) Vertical trench gate type SiC MOSFET. Reproduced from [34]. © IOP Publishing Ltd All rights reserved.

that may produce the same device characteristics and performance compared to a real p-type layer. It is believed that such a resistive layer can block high voltages and current levels during off-state if designed properly [44, 45], making it indistinguishable from a p-type layer from a circuit-level perspective. Such a resistive layer that replaces the functionality of a p-layer is called a 'current blocking layer' (CBL) in general.

Out of the three solutions that have emerged for $Ga_2O_3$ vertical transistors, the CBL type MOSFET resembles closest to commercial SiC and Si power devices structurally which do not require heterogeneous integration of other materials or small critical dimensions in the channel region. Therefore, it has a strong potential to deliver high-performance and low-cost $Ga_2O_3$ vertical switches that can directly compete with SiC devices if successful. In particular, the successful implementation of diffusion doping in $Ga_2O_3$ could mark a paradigm shift for the next generation of power device technology. Therefore, in this perspective, vertical $Ga_2O_3$ MOSFETs utilizing the current blocking layer will be examined with a special focus on Mg diffusion-doped CBL.

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## 2. Current status of vertical $Ga_2O_3$ MOSFETs utilizing current blocking layer

Many methods to introduce CBL in the $Ga_2O_3$ epitaxial layer are somewhat by-products of the attempts to create p-type layers in $Ga_2O_3$. It has been experimentally reported that Mg, N, and Fe, out of many other potential dopants, can all induce a resistive layer in $Ga_2O_3$ that is indicated by a low electron density and high resistivity [46–52]. From a traditional p-type doping perspective, the blocking capability of the CBL could be dictated by various factors, including the dopant species, its density, the doping method, and the activation efficiency. Theoretical calculations have shown that Mg and N are the most probable p-type dopants for $Ga_2O_3$ due to their relatively low formation energies and activation energies [53–56]. Therefore, most efforts for CBL doping have been made towards incorporating N and Mg into $Ga_2O_3$ epitaxial layers with commonly used methods such as epitaxial doping (with MOCVD and MBE) [49], ion implantation [52] , and diffusion doping [57]. In addition to the widely used doping methods, CBL can also be induced simply by manipulating the density of different defects in $Ga_2O_3$ via thermal annealing processes. In particular, it is reported that oxygen annealing [31, 39, 50, 58] of $Ga_2O_3$ under certain conditions can significantly increase the gallium vacancy population, which is demonstrated to drastically reduce the electron density, leading to the creation of a CBL near the surface.

Utilizing the versatile MOCVD and MBE epitaxial growth methods, controllable N and Mg doping have been successfully demonstrated [49, 59–61]. However, no devices utilizing these CBLs have been reported until very recently [62]. The limited electrical measurements on MOCVD-grown Mg-doped CBLs [49, 61] showed a maximum blocking voltage of 100 V with 250 nm of $8.25 \times 10^{17}$ $cm^{-3}$ Mg-doped CBL, resulting in a maximum blocking field of 4 MV $cm^{-1}$. More importantly, the experiment showed a clear trend where a higher Mg doping in the CBL gave it a higher blocking voltage/ field. However, all the blocking *IV* data showed an early onset of high leakage currents, which can indicate an inefficient blocking or trapping of electrons in these layers. In the recent U-Trench gate MOSFET demonstration by Saha *et al* [62], with a high MOCVD Mg concentration of $1.3 \times 10^{19}$ $cm^{-3}$, the blocking voltage of a 200 nm CBL is measured to be ~100 V.

### 2.1. Vertical MOSFET with N-doped CBL

Using the commercially available high-quality HVPE-grown Si-doped $Ga_2O_3$ epitaxial wafers, ion-implantation of Mg and N into the wafer has been demonstrated. However, the activation annealing required for crystal recovery following the implantation of Mg inevitably caused diffusion of Mg due to its high diffusivity in $Ga_2O_3$, smearing out its dopant profile. In most cases, the Mg falls back to the Si background doping level regardless of the intended doping density. For a $2 \times 10^{16}$ $cm^{-3}$ Si-doped epitaxial layer, this means the Mg doping density will be approximately $2 \times 10^{16}$ $cm^{-3}$ as well after the post-implant annealing, even though the initial Mg chemical concentration is 100 times higher immediately following the ion-implantation. Such behavior is fundamentally the result of the high diffusivity of Mg in $\beta$-$Ga_2O_3$ and can be difficult to overcome.

On the other hand, the diffusion of N is relatively low in $Ga_2O_3$ under 1200 °C, leaving a large room for post-implantation annealing. During the annealing, the $Ga_2O_3$ crystal structure recovers, and the N is also activated, signified by the reduction of leakage current through the N-implanted CBL. While Mg-implanted CBL gives virtually no blocking, the N-implanted CBL was able to block >200 V in the same

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set of experiments. Utilizing N-implanted CBL, Wong and Higashiwaki demonstrated the first all-planar $Ga_2O_3$ current aperture vertical-electron-transistor (CAVET), shown in figure 4, with a decent on/off ratio of $10^7$ and a breakdown voltage of 263 V, validating the viability of such methods [63]. The CBL is formed by a single implant of N at 480 keV, resulting in a 0.8 $\mu$m deep junction with a peak N concentration of $1.5 \times 10^{18}$ $cm^{-3}$. This is followed by an optimized post-implant annealing at 1100 °C in $N_2$ for 30 min. However, similar to the MOCVD Mg-doped CBL, the blocking *IV* characteristic also showed an early onset of high leakage current, which seems to be a common theme among vertical $Ga_2O_3$ utilizing CBLs.

Ma *et al* utilized a U-trench gate structure combined with a similar N-implanted CBL process for the vertical MOSFET [40] and were able to achieve a higher breakdown voltage at 534 V and a peak current of 702.3 A $cm^{-2}$ (figure 5). It is also observed that a higher N implant concentration led to a lower leakage current in the CBL and ultimately contributed to a higher breakdown voltage. Nevertheless, due to the large leakage current during the off-state. The on/off ratio in the MOSFET is measured to be $<10^5$. In the latest development, Liu *et al* demonstrated a significantly improved breakdown voltage of >1 kV in a vertical UMOSFET with N-implanted CBL [38]. This is likely attributed to a combination of multiple (5) implants of Nitrogen with the highest energy dose at 680 keV, resulting in a peak N concentration of $1.5 \times 10^{18}$ $cm^{-3}$ and optimized post-implant annealing conditions. In its blocking *IV* characteristics, the leakage current again rises quickly after 0 V, which might become large when the device area is scaled up aggressively. To address the high leakage problem, high temperature (HT, 500 °C) N-implanted CBL was investigated by Hu *et al* [64]. Compared with room temperature N-implant with post-implant annealing, HT implant has reduced crystal damage during the annealing, while maintaining a good surface morphology and achieving a higher activation efficiency, resulting in $a \sim 4$ orders of magnitude lower leakage current in the CBL.

In addition to the N-implanted CBL, MOCVD-grown N-doped CBL is also gaining attention recently. Alema *et al* demonstrated controllable N doping using $NH_3/N_2$ as the source in an MOCVD system [59]. The doping can be modulated by the flow rate within the range of $1 \times 10^{18}$ $cm^{-3}$ to $2 \times 10^{20}$ $cm^{-3}$. The growth is done on an Fe-doped $\beta$-$Ga_2O_3$ substrate, as such, the *IV* blocking characteristic is not measured. On the other hand, Xu *et al* utilized $N_2O$ as the dopant source, achieving a similar doping range [65]. The N-doped CBL is re-grown on a 10 $\mu$m HVPE commercial wafer. Therefore, they were able to demonstrate the blocking capability of the MOCVD-grown N-doped CBL with a Schottky barrier diode ( SBD)-like structure having the blanket CBL present at the surface, as shown in figure 6(a). This effectively rendered the

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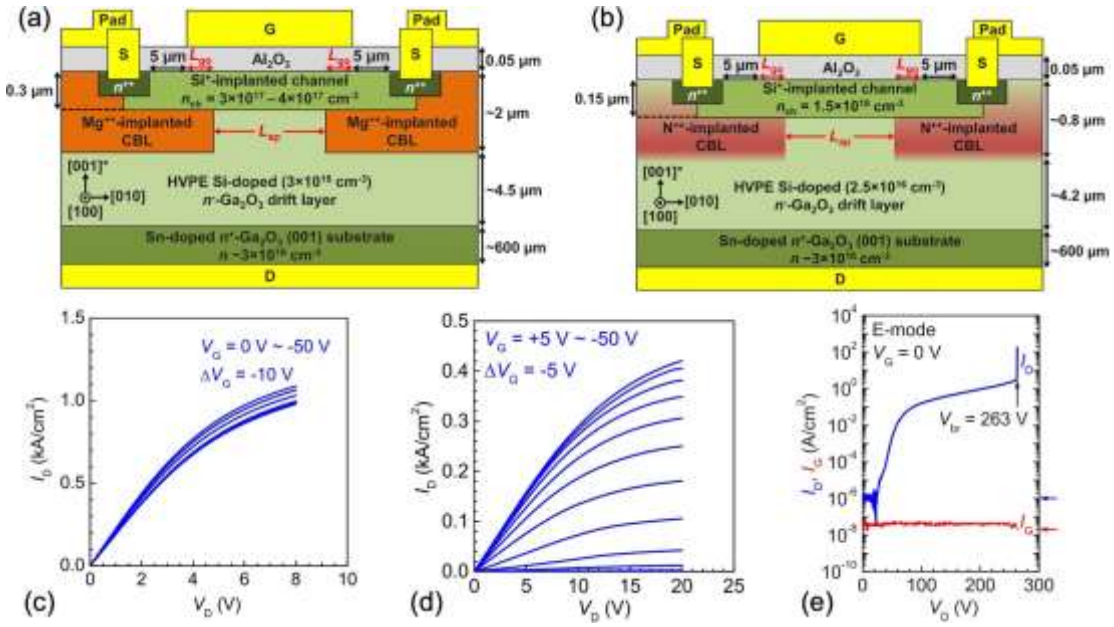


**Figure4.** Cross-section schematics of $Ga_2O_3$ (a) CAVETwith Mg implanted CBLand (b) CAVETwith N implanted CBL;output *IV* characteristics of (c) CAVETwith Mg implanted CBLand (d) CAVETwith N implanted CBL;(e) breakdown characteristic of enhancement mode CAVETwith N implanted CBL.© 2020 IEEE.Reprinted, with permission, from [63].

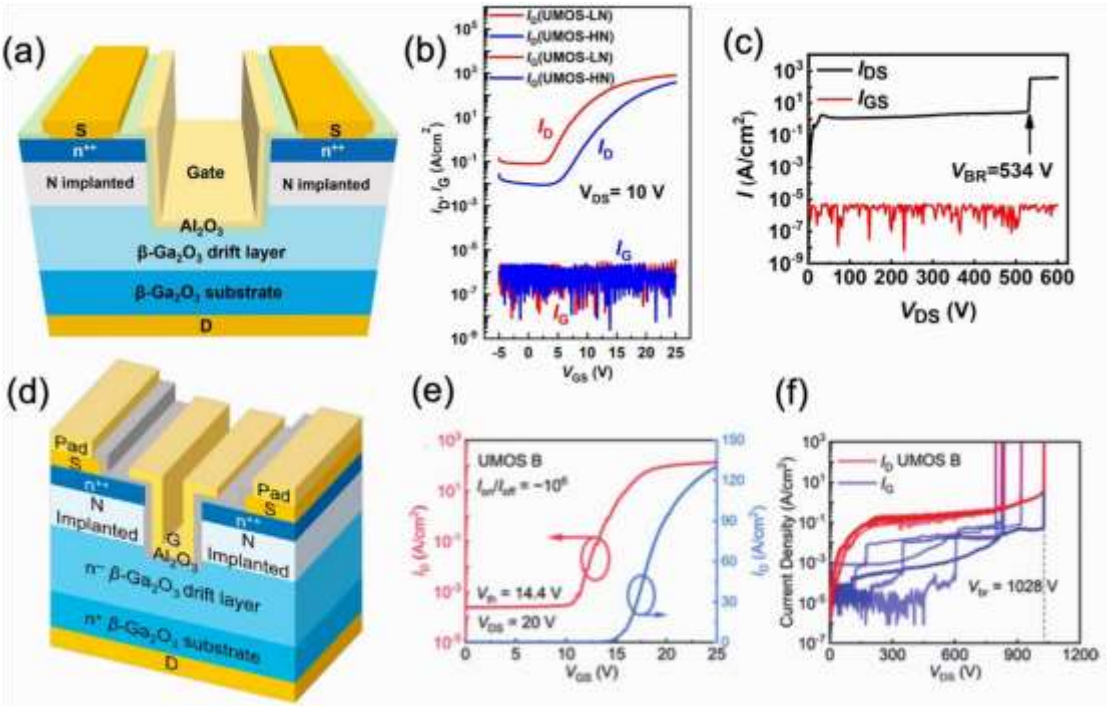


**Figure5.** Cross-section schematics of $Ga_2O_3$ U-Trench gate MOSFETwith (a) shallower N-implanted CBLand (d) deeper N-implanted CBLwith optimized post implant annealing; the output and breakdown *IV* characteristics of (a) is shown in (b) and (c); the output and breakdown *IV* characteristics of (d) is shown in (e) and (f). (a)–(c) © 2023 IEEE.Reprinted, with permission, from [40]. (d)–(f) © 2024 IEEE.Reprinted, with permission, from [38].

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initial diode insulating in both forward and reverse directions. The bi-directional blocking voltage is more than 3.5 kV for a 1 $\mu$m CBL with a low nitrogen doping of <4.3 × $10^{17}$ $cm^3$ grown at 1100 °C. It is worth noting that the leakage in this case is much lower than the N-implanted CBL described above, giving a current on/off ratio comparable to normal power devices. This seems to suggest that the MOCVD doped nitrogen CBL is much more effective in blocking the current than the N-implanted one. However, this doping method is not selective, necessitating etching through the CBL to form the channel.

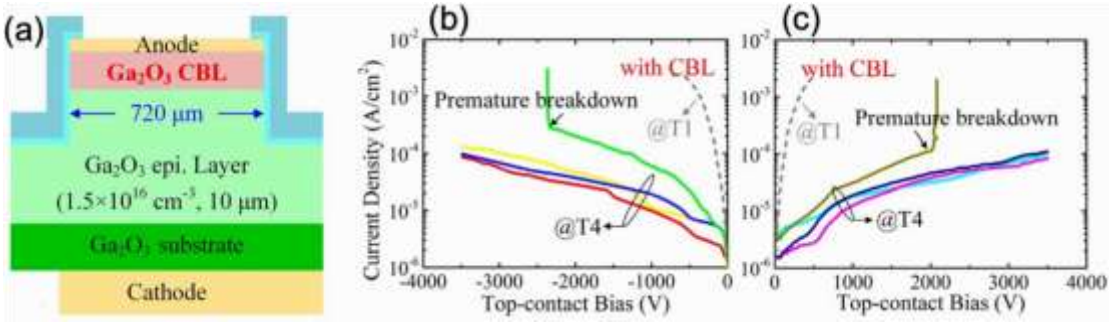


**Figure6.** (a) Cross-section schematics of the MOCVD N-doped $Ga_2O_3$ CBL test structure. (b) Its reverse and (c) forward biased *IV* characteristic. Reprinted from [65], with the permission of AIP Publishing.

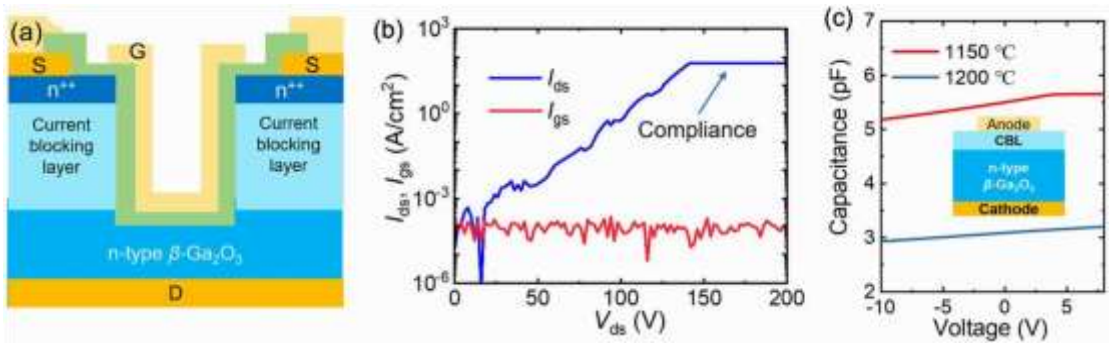


**Figure7.** (a) Cross-section schematics of $Ga_2O_3$ U-Trench gate MOSFET with oxygen annealed CBL and (b) its breakdown characteristics. (c) Showcases the effect of oxygen annealing depleting the drift layer via CV measurement of shown diode structure. Reprinted from [39], with the permission of AIP Publishing.

## 2.2. Vertical MOSFET with oxygen annealed CBL

Early on during the $Ga_2O_3$ device research, oxygen annealing (OA) has been reported to significantly reduce the conductivity of bulk $Ga_2O_3$ wafers during growth. It is later shown that intentional OA treatment can also induce a highly resistive layer in the epitaxial wafers and thus can be used for creating CBL in vertical MOSFETs. It is speculated that exposure to oxygen at elevated temperatures significantly increases the gallium vacancy population in $\beta$-$Ga_2O_3$. These vacancies effectively capture electrons and thus are responsible for the reduction of conductivity in the $Ga_2O_3$. One of the advantages of the oxygen annealing method compared to extrinsic doping with ion implantation is that the crystal damage is relatively low.

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Zhou *et al* demonstrated the first of such devices by annealing HVPE $\beta$-$Ga_2O_3$ samples at 1200 °C in an oxygen atmosphere for 6 h [39]. The device is fabricated with a U-shaped gate trench for enhancement operation, as shown in figure 7(a). The UMOSFET achieved a large threshold voltage of 11.5 V, a maximum on-state current of 11 A $cm^{-2}$, and a current on/off ratio of 6 × $10^4$. The device is again plagued by a large leakage current immediately after the voltage ramp, measuring a breakdown around 100 V.

It is worth noting that the intriguing demonstration of the blocking capability of OA-CBL here, as well as in many other reports, validated the potential of this method for modifying the electrical behavior of $Ga_2O_3$. The OA technique is used in several demonstrations on ultra-high voltage $Ga_2O_3$ diodes [26, 66], which utilized it to reduce the carrier concentration in the drift layer, effectively surpassing the leakage current and increasing the electric field strength and breakdown voltages in the same layer. The OA process was also reported to increase the blocking capability of MOCVD-grown N-doped CBL by modulating certain deep traps and the related charge density [67]. The successful implementation of the OA technique collectively has inspired the effort of OA-assisted Mg diffusion doping described in the next section, resolving one of the most critical challenges in diffusion doping of Mg in $Ga_2O_3$.

**2.3. Vertical MOSFET with Mg diffused CBL vertical diffused barrier field-effect-transistor ( VDBFET )** Among the three primary semiconductor doping technologies, diffusion doping has historically fallen out of favor due to the lack of precise control over the doping profile. This is worsened by more complex reactions happening in compound semiconductors at high temperatures that cause non-uniformity and create defects in the crystal structure during the diffusion process. For the mature silicon carbide (SiC) technology, due to

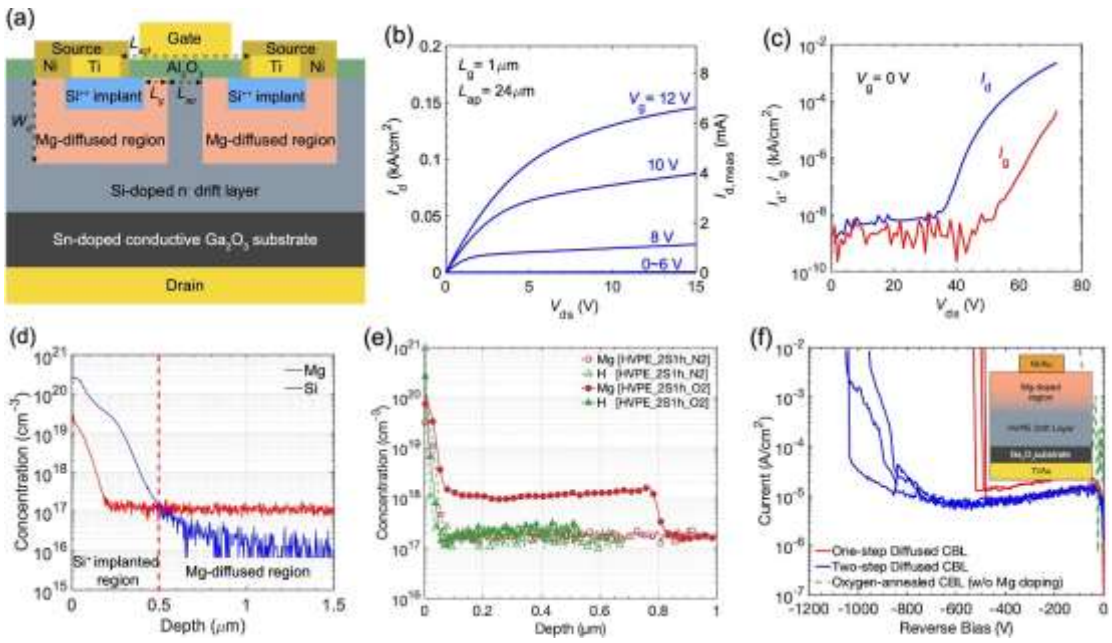


**Figure8.** $Ga_2O_3$ VDBFET's (a) cross-section schematic, (b) output *IV* characteristics, (c) breakdown characteristics, and (d) SIMS Si and Mg dopant profiles from the surface to the CBL region. (e) Showcases the 10 times increased Mg concentration and (d) the resulting increased blocking in CBL measured in the inset diode structure. (a)–(c) © 2022 IEEE. Reprinted, with permission, from [43]. (d)–(f) Reprinted from [57], with the permission of AIP Publishing.

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the exceptionally low diffusion constants of the n and p-type dopants, diffusion doping becomes practically improbable. However, for $Ga_2O_3$, the situation is very different: First, the diffusivity of desired dopants in $Ga_2O_3$ is relatively high under reasonable temperatures (900 °C–1200 °C) [68]; Second, $\beta$-$Ga_2O_3$ itself, as an ultra-WBG material, is naturally more stable under high temperatures. The unique combination of the physical properties in gallium oxide makes diffusion doping an attractive option again.

Utilizing the furnace anneal thermal diffusion method, coupled with a selective Mg diffusion doping technique, a Mg diffused CBL is realized in a commercial HVPE-grown Si-doped $Ga_2O_3$ epitaxial wafer [43]. An all-planar enhancement mode vertical MOSFET is demonstrated with drastically reduced fabrication steps compared to N-implanted CAVET. The device, shown in figure 8(a), is properly named 'VDBFET', describing its processing techniques. Because the diffused Mg naturally compensates the electrons at the surface, a normally-off device is formed without additional steps. The VDBFET featured a turn-on voltage of ~7 V, a high on/off ratio of $10^9$, and a decent saturation with an on-current of 150 A $cm^{-2}$. However, the breakdown voltage is measured to be around 72 V. This is caused by a lower-than-expected Mg doping concentration in the CBL, indicating a lack of Mg doping control for the diffusion doping method, which is the main drawback of the diffusion doping method in general historically. Utilizing the same process as an edge termination technique in $Ga_2O_3$ SBD, Li *et al* demonstrated a remarkable increase of breakdown voltage from 580 V to 2.2 kV without sacrificing specific on-resistance of the device [69]. This further showcases the efficacy of the Mg diffusion doping and its applications in other scenarios.

A recent breakthrough report addressed the low Mg diffusion doping problem by leveraging oxygen annealing in the diffusion doping process [57]. It is observed that by introducing oxygen during the high-temperature diffusion annealing, the Mg concentration is seen to have increased by nearly ten times in the CBL. It is believed that the introduction of oxygen during the high-temperature processing again induced a large population of gallium vacancies. These gallium vacancies are immediately filled by Mg that was driven in from a surface dopant source. This theory also indicates that the OA-generated gallium vacancy population is at least ten times higher than the original Mg doping concentration when oxygen is not involved. The detailed mechanism and a precise method to control Mg doping require further clarification. In the same report, preliminary *IV* data also showed a significantly increased CBL blocking voltage of >1 kV, indicating a positive relation between CBL doping and breakdown voltage. This latest advancement paves the way for the fabrication of high-voltage $Ga_2O_3$ VDBFETs.

## 3. Outlook for the $Ga_2O_3$ VDBFET

In the pursuit of suitable p-type dopants for $Ga_2O_3$, theoretical researchers have meticulously investigated a wide range of potential candidates. Among them, magnesium (Mg) has emerged as the 'optimal acceptor' due to its lowest formation energy and ionization energy. Although first-principle calculations predicted an acceptor ionization energy exceeding 1 eV for Mg, other acceptors like nitrogen and iron exhibit even higher ionization energies. Theoretical studies suggest achieving p-type conduction by alloying $Ga_2O_3$ with different metals to elevate the valence band. In this context, Mg emerges as the most probable acceptor [56]. However, without effective acceptor doping, Mg is likely

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to be the most efficient deep electron trap and thus may be sufficient for the off-state blocking of high-voltage power transistors.

The diffusion doping method and commercial HVPE-grown $Ga_2O_3$ wafers are chosen to be used for the fabrication of VDBFETs. Mg-doped spin-on-glass (SOG) is used in this study and can be treated as an infinite source due to the high concentration. Selective doping can be easily implemented by patterning the SOG with conventional photolithography, making it useful for various device applications. The diffusion doping method is utilized for Mg doping in $Ga_2O_3$ to take advantage of its high diffusivity, which is dictated by the physical property of $Ga_2O_3$. Among the available $Ga_2O_3$ epitaxial layers, commercial HVPE wafers have some of the lowest defect densities and highest crystal qualities [1]. The diffusion process is known to be significantly affected by the defect's characteristics in the wafer. As a result, previous diffusion doping efforts in other compound semiconductors were severely hindered by the inconsistent quality of the epitaxial wafers. In contrast, the availability of high-quality commercial $Ga_2O_3$ wafers now has enabled a more isolated study of diffusion doping in this material, providing a valuable opportunity to gain insights into its diffusion behavior. This also gives us the best chance to realize high-efficiency Mg doping. Furthermore, the diodes fabricated using commercial HVPE wafers have achieved remarkable results, approaching the fundamental limits of $Ga_2O_3$. Consequently, successful doping and devices fabricated from these wafers hold great promise for delivering low-cost high-voltage vertical $Ga_2O_3$ transistors.

### 3.1. Enhancement-mode (normally-off) operation

All planar enhancement mode MOSFETs can be easily achieved with Mg diffusion doping due to the high Mg doping at the surface. These Mg dopants effectively compensate electrons in the CBL region and at the surface, creating a depletion region at equilibrium. Luckily, the Fermi level in the highly Mg-doped region is not pinned and can be easily modulated by the gate voltage. When a large positive voltage is applied to the gate, a conductive surface electron channel is formed to allow for current flow. This behavior is similar to the conventional inversion operation observed in p-layers under the gate. Thus, the CBL can be considered a quasi-p-type layer, allowing for the realization of quasi-inversion-mode operation that eliminates the trade-off between high current density and large positive threshold voltage ($V_T$). In electrical systems, due to safety reasons, enhancement-mode operation is always preferred. Mg diffusion doping provides an easy and effective method to achieve this goal. It is also worth noting that, after diffusion doping, all samples maintained a pristine surface indistinguishable from a new wafer. This allows for uninterrupted device fabrication following the process, free from any surface roughness or degradation issues.

However, there is a significant trade-off between the enhancement mode operation and high channel mobility due to the surface scattering of channel electrons. Device designers have a choice between using an inversion channel, where electron channel is formed in response to the positive gate bias thus are confined to the gate oxide-channel interface (enhancement-mode), or an accumulation channel, where channel already exist at zero gate bias and the electrons are further away from the interface (depletion-mode). The first VDBFET demonstration showed an enhancement-mode or normally-off operation with an estimated channel mobility of 7.5 $cm^2 V^{-1} \cdot s^{-1}$ without any targeted optimization. It is expected that future optimization will bring the inversion channel mobility up to a level close to the

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SOA SiC ones. As shown in figure 9(a), the channel resistance dominates the overall device on-resistance ($R_{ON}$) for low-voltage (<1 kV) vertical FETs because the drift layer thickness is close to the gate length, thus drift resistance is negligible compared to the channel resistance. In this case, the lateral depletion-mode device has an advantage due to the high channel mobility. However, as the voltage rating scales up (~2 kV), more drift thickness is needed, lateral device drift resistance increases drastically, and vertical device $R_{ON}$ are much smaller in comparison due to the current spreading in the drift layer. Furthermore, lateral devices experience severe extrinsic breakdown effect (air arcing, interface-related leakage, etc) that further lowers the breakdown voltage and translates into a higher $R_{ON}$ for a given drift thickness. Therefore, vertical FETs with either inversion-type or

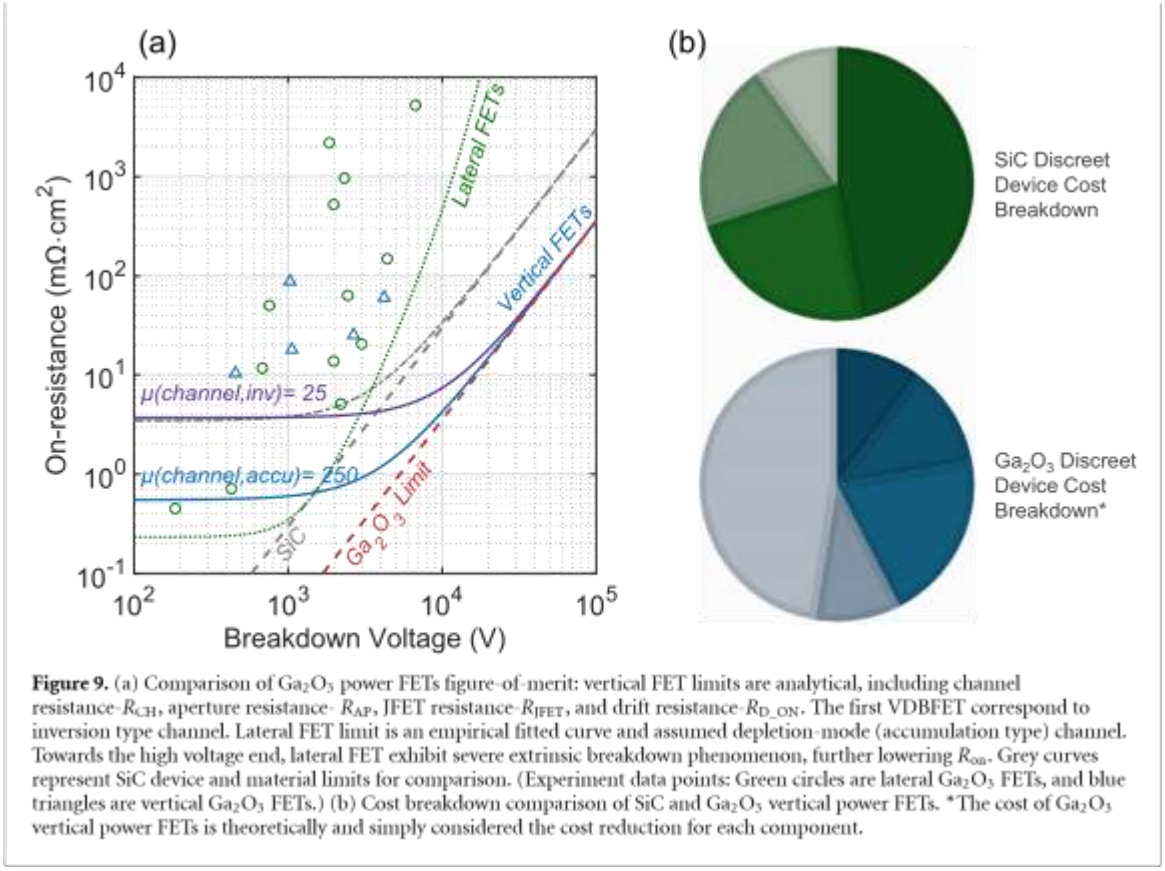


**Figure 9.** (a) Comparison of $Ga_2O_3$ power FETs figure-of-merit: vertical FET limits are analytical, including channel resistance-$R_{CH}$, aperture resistance- $R_{AP}$, JFET resistance-$R_{JFET}$, and drift resistance-$R_{D\_ON}$. The first VDBFET correspond to inversion type channel. Lateral FET limit is an empirical fitted curve and assumed depletion-mode (accumulation type) channel. Towards the high voltage end, lateral FET exhibit severe extrinsic breakdown phenomenon, further lowering $R_{on}$. Grey curves represent SiC device and material limits for comparison. (Experiment data points: Green circles are lateral $Ga_2O_3$ FETs, and blue triangles are vertical $Ga_2O_3$ FETs.) (b) Cost breakdown comparison of SiC and $Ga_2O_3$ vertical power FETs. *The cost of $Ga_2O_3$ vertical power FETs is theoretically and simply considered the cost reduction for each component.

accumulation-type channel will be the only viable solution for high and ultra-high (>10 kV) voltage high-efficiency $Ga_2O_3$ power devices.

### 3.2. Ultra-low leakage off-state

One of the great benefits of diffusion doping is that the process does not cause severe crystal damage, as seen in the implantation process. Thus, a highly efficient Mg diffused doping should yield an extremely low leakage current and high breakdown. This is indicated by the high on/off ratio of $10^9$ in the first VDBFET. Although the channel leakages in VDBFET started rising after 40 V, it is speculated that this only happened due to the lower-than-expected Mg doping density and not because of the inefficiency of Mg in capturing the electrons, i.e. CBL's blocking efficiency. Furthermore, it is reported that the low Mg doping in the CBL of the VDBFET is not even fully activated due to the Mg–H complex.

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The oxygen annealing during the Mg drive-in diffusion step has achieved a simultaneous increase of Mg doping by ten times and the dissociation of the Mg–H complex in the CBL, which is indicated by the clear separation of Mg and H in the SIMS profile shown in figure 8(e). It is also believed that Mg, in this case, occupied the gallium vacancies generated by the oxygen annealing, which means Mg doping is substitutional instead of interstitial. This will contribute to a high activation ratio for Mg dopants, resulting in a high-efficiency Mg-doped CBL. These factors together are likely to drastically reduce the leakage current until near the breakdown voltage.

In addition, deep and uniform junctions can be formed with a simple two-step oxygen-assisted Mg diffusion doping instead of multiple implants, especially needed for super-junction-based devices. One of the most striking features of the oxygen-assisted Mg diffusion doping technique is that it produces an extremely flat Mg doping profile that is indistinguishable from the doping profiles of epitaxial growth methods such as MOCVD and MBE. This highly desired profile is somewhat unexpected and a significant departure from the traditionally observed Gaussian-like profiles from diffusion doping. Even with ion implantation, to achieve such a flat profile over a large depth, a combination of many implantations is required. This unique advantage makes OA Mg diffusion doping especially interesting and useful for device applications. Moreover, our preliminary data shows that a 1 hour 1000 °C Mg diffusion can penetrate at least 10 $\mu$m into the $Ga_2O_3$ substrate, such speed is way above the limit of MOCVD growth, and the depth is way above what is achievable via ion-implantation. Such ultra-deep junction is required for super-junction devices, which can extend the voltage rating of power diodes and transistors to their absolute maximum. Besides, it is also essential for an ultra-high-voltage device to have a p-body layer that is deep enough to balance the excessive charges in the thick drift layer depletion region. Consider another case where the CBL without mobile holes is actually acting as depletion layer itself, instead of depleting the drift layer beneath, (which is confirmed by some CV measurements) an extra thick Mg CBL will nevertheless contribute to a lower leakage current and better blocking by shielding the channel from the high electric field in the drift region.

### 3.3. High off-state breakdown voltage

Similar to what's observed in conventional p-type doping, the breakdown voltage in the vertical transistors is strongly dependent on the p-layer dopant density and thickness. It has been reported in MOCVD-grown Mg-doped CBLs in $Ga_2O_3$ that a higher Mg doping resulted in a higher blocking, in agreement with conventional wisdom. In Mg-diffused CBL, the same phenomenon is also observed. With a Mg doping of $1 \times 10^{17}$ cm$^{-3}$, the first VDBFET measured a blocking voltage of ~72 V. However, with an increase of Mg doping by ten times, the blocking in the CBL has increased to nearly 1 kV. The remarkable increase of blocking voltages with higher Mg doping shown in figures 8(e) and (f) strongly suggests that such a trend can be extended further. It is likely that with oxygen annealing optimization, the Mg doping in the CBL can be increased to more than $1 \times 10^{19}$ cm$^{-3}$. Due to the proposed OA-assisted highly efficient Mg doping, this CBL will likely exhibit a high blocking capability among all possible CBL strategies in $Ga_2O_3$. A distinctive advantage of oxygen annealing is its ability to simultaneously increase Mg doping during the drive-in process while disassociating Mg–H complexes within $Ga_2O_3$. Combined with a decent $1 \times 10^{18}$ cm$^{-3}$ Mg doping, we observed some of the highest blocking voltages measured in a vertical CBL in $Ga_2O_3$. Furthermore, during breakdown measurement, Mg-CBL showed an extremely

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low leakage current, maintaining a $10^9$ on/off ratio until the soft breakdown. It is hypothesized that the high leakage has stemmed from inefficient carrier trapping in these alternative CBLs. Therefore, an OA-assisted Mg-diffused CBL with doping of $1 \times 10^{19}$ $cm^{-3}$ will likely produce a high-voltage VDBFET with ultra-low leakage during the off state.

An effective and tunable Mg-doped CBL can not only serve to replace the p-body layer in vertical FETs but also provide the ultimate edge termination for high-voltage devices, which can significantly improve its reliability. This is partly manifested as a low off-state leakage current, as detailed in the last section. High-voltage device isolation is usually achieved via field shielding provided by the highly p-type doped region, such as junction termination extension [70, 71]. The ultra-deep highly diffusion-doped Mg region can be used as an effective edge termination structure surrounding the active region and below the field plates. Combined with field plating techniques, it is likely to extend the voltage rating of CBL-based vertical $Ga_2O_3$ FETs well into the ultra-high voltage (>10 kV) ranges.

### 3.4. Soft-breakdown

Because the Mg-CBL is formed spontaneously during a non-invasive thermal diffusion process, its interface with the $n^-$ layer underneath is almost free of any defects and damages, and buried deep within the epitaxial layer, microns away from the surface. Therefore, extrinsic breakdown effects such as air arcing and surface leakages are largely suppressed. The intrinsic breakdown or leakage through the CBL will likely take over well before the extrinsic breakdown. This is opposite to what's observed routinely in lateral devices and confirmed by the non-destructive breakdown *IV* measurement in the VDBFETs and Mg diffused CBLs up to 1 kV. In lateral device breakdown measurements, even when the device is submerged in Fluorinert to prevent air arching, the device will most likely not survive after the first successful attempt. In most cases, the electric field peak at the gate near the channel surface will cause a premature surface breakdown in this region, characterized by explosive destruction of the gate contact shown in figure 10(b). This will render the device useless right away. It is unlikely that $Ga_2O_3$ lateral transistors will survive such extreme conditions. However, in vertical MOSFETs, the breakdown measurement can often be repeated many times depending on the current compliance and device structures. After the first breakdown measurement, the blocking voltage can experience a moderate drop of 30%–40% but will slowly recover over time. Destruction in vertical FETs is much less likely, even in these initial experiments, due to the buried CBL structures, shown in figure 10( c ). This characteristic is desired for high-power applications where high reliability is desired. In theory, the soft-breakdown behavior can also provide a larger current surge capacity during transient, similar to an avalanche. However, this phenomenon needs to be further investigated, and proper engineering in the CBL may push its performance very close to the avalanche limit, in which case, the reliability becomes a significant concern.

The reliability of the device under high power stress mainly considers the breakdown ruggedness and thermal effects of the device. In principle, the ultra-WBG nature of $\beta$-$Ga_2O_3$ itself already provides a large safety margin for high-power reliability concerns. For thermal effect, vertical devices provide maximum current spreading and volumetric 3D heat dissipation, coupled with device-level (CVD diamond heat sink [72], etc) thermal management and SOA thermal packaging (double-side cooling, nanosilver sintering, etc), the low thermal conductivity problem can be largely alleviated even under

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high current avalanching conditions [73]. On the other hand, the Mg CBL can provide great design flexibility in terms of edge

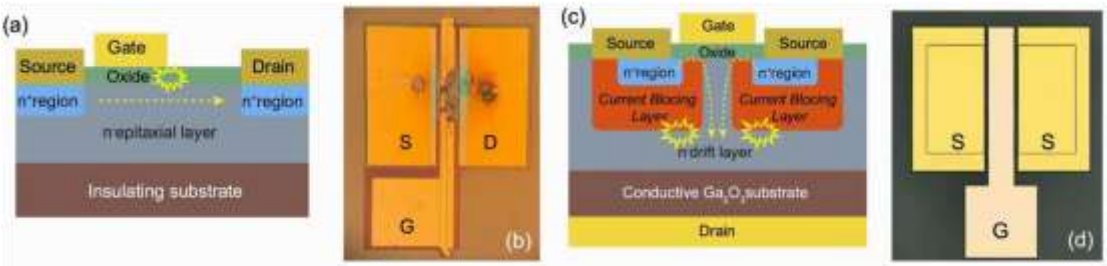


**Figure10.** (a) Cross-section schematic, and (b) optical image of a lateral MOSFET after breakdown [10]; (c) cross-section schematic, and (d) optical image of the VDBFET.The breakdown showcased in (b) is measured inside the Fluorinert liquid. It can be seen that the explosion happened at the gate electrode edge towards the drain side, where the electric field peak is expected. The two smaller explosion craters at the source and drain pad is the result of high surge current after the shorting of device terminals after high voltage breakdown. Such destructive behavior is less likely in vertical devices.

termination, field shielding, and charge balancing, reducing the edge and bulk leakage related to defects, which in principle, minimizes the likelihood of high-field breakdown failure. In particular, the VDBFET, with an all-planar structure having minimum fabrication complexity, a buried gate barrier, no gate etching or sharp geometries, will ensure a high device structure integrity and reliability, less prone to fabrication process-related instability and parameter shifts. However, there is still a lack of experimental reliability data on the Mg-doped CBL and devices.

### 3.5. Fast switching

Perhaps the biggest operational difference between a VDBFET and a traditional VDMOS transistor lies in the difference between the CBL and the real p-type layer. In the VDMOS, with a conducive p-layer, there always exists a body diode between the p-layer and the underneath n-type drift layer. However, in VDBFET, because the CBL is non-conductive, the body diode does not exist, which eliminates the slow reverse recovery stemming from slow-responding holes. The recently published static *IV* measurement showed that the diffused Mg CBL blocks in both forward and reverse directions up to hundreds of volts [57]. The absence of slow responding holes in the Mg-doped CBL in $Ga_2O_3$ may turn out to be an advantage during fast switching. In this case, electron trapping and detrapping may play a decisive role in the switching speed. For proper operation, an external free-wheeling diode needs to be added for switching measurements. Nevertheless, the switching characteristics of CBL-based $Ga_2O_3$ vertical transistors remain unknown due to the early development stage of this technology.

### 3.6. Challenges

The ability to precisely control the doping profile (density and depth) via diffusion has long been the main challenge for this method. However, it has been demonstrated that oxygen annealing can effectively increase the doping density by ten times to $\sim 1 \times 10^{18}$ $cm^{-3}$. What is the upper limit of this method? And is it enough for ultra-high voltage operation? remains unknown. In addition, what would be the conditions and techniques required to achieve such a high degree of control are yet to be discovered. Nevertheless, the data so far has shown that several kV operation can be realized with the CBL base MOSFET, and the trend points to a highly encouraging outlook. The reproducibility and lateral diffusion problem are also among its biggest downfalls, which can be easily compensated by

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mask design and structure optimizations, given that power devices are usually large enough that it does not require extremely high precision with device dimensions.

The absence of mobile holes in the p-layer gives rise to several unconventional physical problems. Because the entire Mg CBL region is not conductive, it is essentially a 'dead zone' without any carriers at all and behaves like a depletion region instead of a p-layer. Therefore, the buried CBL is not internally electrically connected to the source electrode and thus would not hold the same ground potential as the source, even if it is connected to the source at the surface. In principle, this makes the electric field distribution significantly different from what's observed from traditional n–p–n layers and may create field peaks at different locations. This may require new field management and edge termination techniques specifically designed for such structures. In addition, the potential barrier between the n layer and CBL is much lower than that of a traditional pn junction, in principle. However, owing to the large bandgap of $Ga_2O_3$, a potential barrier equivalent to the partial bandgap of $Ga_2O_3$ can still be larger than the entire bandgap of Si, thus can still yield strong current blocking capability. The specific barrier height would largely depend on the activation of Mg dopants and their density and would require a detailed study into the fundamental physics of diffused Mg dopants.

## 4. Conclusion

Vertical $Ga_2O_3$ MOSFET that utilizes CBL for off-state blocking is still an active research topic that requires significant advancement and broader participation. Among the many potential CBL dopants and doping methods, N implantation so far has exhibited the best performance. However, because of the promising property of the Mg dopant in $Ga_2O_3$, effective Mg doping via diffusion method holds the potential for enabling high voltage and high power operation with minimal processing complexity. The diffusion doping method alone has been proven to be a simple yet effective doping tool with high device fabrication compatibility. Although true p-type doping in $Ga_2O_3$ remains unlikely, highly efficient CBL that can sustain high voltages may hold the key to realizing low-cost, high-power, and high-efficiency $Ga_2O_3$ vertical transistors that can revolutionize power electronics in the coming decades.

## Data availability statement

No new data were created or analysed in this study.

## References

Green A J *et al* 2022 β-Gallium oxide power electronics *APL Mater.* **10** 029201

Higashiwaki M and Jessen G H 2018 Guest Editorial: the dawn of gallium oxide microelectronics *Appl. Phys. Lett.* **112** 060401

Pearton S J *et al* 2018 A review of $Ga_2O_3$ materials, processing, and devices *Appl. Phys. Rev.* **5** 011301

Zhang R *et al* 2024 From wide to ultrawide-bandgap semiconductors for high power and high frequency electronic devices *J. Phys. Mater.* **7** 022003

Mastro M A, Kuramata A, Calkins J, Kim J, Ren F and Pearton S J 2017 Perspective—opportunities and future directions for $Ga_2O_3$ *ECS J. Solid State Sci. Technol.* **6** P356–P9

Vol. 13 No. 1 | Imp. Factor: 8.13
DOI: https://doi.org/10.5281/zenodo.15845908

Tadjer M J 2018 Cheap ultra-wide bandgap power electronics? gallium oxide may hold the answer *Interface* **27** 49–52

Reese S B, Remo T, Green J and Zakutayev A 2019 How much will gallium oxide power electronics cost? *Joule* **3** 903–7

Wong M H, Sasaki K, Kuramata A, Yamakoshi S and Higashiwaki M 2016 Field-plated $Ga_2O_3$ MOSFETs with a breakdown voltage of over 750 V *IEEE Electron Device Lett.* **37** 212–5

Zhou H, Maize K, Qiu G, Shakouri A and Ye P D 2017 β-$Ga_2O_3$ on insulator field-effect transistors with drain currents exceeding

1.5 A/mm and their self-heating effect *Appl. Phys. Lett.* **111** 092102

Zeng K, Vaidya A and Singisetti U 2018 1.85 kV breakdown voltage in lateral field-plated $Ga_2O_3$ MOSFETs *IEEE Electron Device Lett.* **39** 1385–8

Zhang Y, Joishi C, Xia Z, Brenner M, Lodha S and Rajan S 2018 Demonstration of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ double heterostructure field effect transistors *Appl. Phys. Lett.* **112** 233503

Dryden D M *et al* 2022 Scaled T-gate β-$Ga_2O_3$ MESFETs with 2.45 kV breakdown and high switching figure of merit *IEEE Electron Device Lett.* **43** 1307–10

Green A J *et al* 2016 3.8 MV/cm breakdown strength of MOVPE-grown Sn-doped β-$Ga_2O_3$ MOSFETs *IEEE Electron Device Lett.* **37** 902–5

Sharma S, Zeng K, Saha S and Singisetti U 2020 Field-plated lateral $Ga_2O_3$ MOSFETs with polymer passivation and 8.03 kV breakdown voltage *IEEE Electron Device Lett.* **41** 836–9

Liu H, Wang Y, Lv Y, Han S, Han T, Dun S, Guo H, Bu A and Feng Z 2023 10 kV lateral β-$Ga_2O_3$ MESFETs with B ion implanted planar isolation *IEEE Electron Device Lett.* **44** 1048–51

Mun J K, Cho K, Chang W, Jung H-W and Do J 2019 Editors' choice—2.32 kV breakdown voltage lateral β-$Ga_2O_3$ MOSFETs with source-connected field plate *ECS J. Solid State Sci. Technol.* **8** Q3079–Q82

Lv Y *et al* 2019 Enhancement-mode β-$Ga_2O_3$ metal-oxide-semiconductor field-effect transistor with high breakdown voltage over 3000 V realized by oxygen annealing *Phys. Status Solidi* **1900586** 1–5

Vol. 13 No. 1 | Imp. Factor: 8.13
DOI: https://doi.org/10.5281/zenodo.15845908

Hu Z *et al* 2018 Field-plated lateral β-$Ga_2O_3$ Schottky barrier diode with high reverse blocking voltage of more than 3 kV and high power figure-of-merit of 500 MW/cm² *IEEE Electron Device Lett.* **39** 1564

Yang J, Ren F, Tadjer M, Pearton S J and Kuramata A 2018 2300V reverse breakdown voltage $Ga_2O_3$ Schottky rectifiers *ECS J. Solid State Sci. Technol.* **7** Q92–Q96

Bhattacharyya A, Ranga P, Roy S, Peterson C, Alema F, Seryogin G, Osinsky A and Krishnamoorthy S 2021 Multi-kV class β-$Ga_2O_3$ MESFETs with a lateral figure of merit up to 355 MW/cm² *IEEE Electron Device Lett.* **42** 2021–4

Sundaram P P, Alema F, Osinsky A and Koester S J 2022 β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure Schottky diodes for improved V BR2/ R ON *J. Vac. Sci. Technol. A* **40** 43211

Kokubun Y, Kubo S and Nakagomi S 2016 All-oxide p-n heterojunction diodes comprising p-type NiO and n-type β-$Ga_2O_3$ *Appl. Phys. Express* **9** 091101

Su C, Zhou H, Hu Z, Wang C, Hao Y and Zhang J 2025 1.96 kV p-$Cr_2O_3$/β-$Ga_2O_3$ heterojunction diodes with an ideality factor of

1.07 *Appl. Phys. Lett.* **126** 132104

Vangipuram V G T, Zhang K, Su Yu D, Meng L, Chae C, Xu Y, Hwang J, Lu W, Zhao H and Phys Lett A 2025 Ultrawide bandgap $LiGa_5O_8$;-$Ga_2O_3$ heterojunction p–n diodes *APL Electron. Devices* **1** 16115

Watahiki T, Yuda Y, Furukawa A, Yamamuka M, Takiguchi Y and Miyajima S 2017 Heterojunction p-$Cu_2O$/n-$Ga_2O_3$ diode with high breakdown voltage *Appl. Phys. Lett.* **111** 222104

Zhang J *et al* 2022 Ultra-wide bandgap semiconductor $Ga_2O_3$ power diodes *Nat. Commun.* **13** 1–8

Dong P, Zhang J, Yan Q, Liu Z, Ma P, Zhou H and Hao Y 2022 6 kV/3.4 mΩ·cm² vertical β-$Ga_2O_3$ Schottky barrier diode with

BV²/Ron,sp performance exceeding 1-D unipolar limit of GaN and SiC *IEEE Electron Device Lett.* **43** 765–8

Roy S, Bhattacharyya A, Ranga P, Splawn H, Leach J and Krishnamoorthy S 2021 High-k oxide field-plated vertical (001) β-$Ga_2O_3$

Schottky barrier diode with Baliga's figure of merit over 1 GW/cm² *IEEE Electron Device Lett.* **42** 1140–3

Qin Y *et al* 2023 10 kV $Ga_2O_3$ charge-balance Schottky rectifier operational at 200 ◦C *IEEE Electron Device Lett.* **44** 1268–71 [30] Ho Q D, Frauenheim T and Deák P 2018 Theoretical confirmation of the polaron model for the Mg acceptor in β-$Ga_2O_3$ *J. Appl. Phys.* **124** 145702

Varley J B, Weber J R, Janotti A and Van De Walle C G 2010 Oxygen vacancies and donor impurities in β-$Ga_2O_3$ *Appl. Phys. Lett.* **97** 97–100

Montgomery R H, Zhang Y, Yuan C, Kim S, Shi J, Itoh T, Mauze A, Kumar S, Speck J and Graham S 2021 Thermal management strategies for gallium oxide vertical trench-fin MOSFETs *J. Appl. Phys.* **129** 85301

Han L, Liang L, Kang Y and Qiu Y 2021 A review of SiC IGBT: models, fabrications, characteristics, and applications *IEEE Trans. Power Electron.* **36** 2080–93

Wang L, Jia Y, Zhou X, Zhao Y, Wang L, Hu D, Wu Y and Deng Z 2021 SiC double-trench MOSFETs with source-recessed structure for enhanced ruggedness *Jpn. J. Appl. Phys.* **60** 124005

Li W, Nomoto K, Hu Z, Nakamura T, Jena D and Xing H G 2019 Single and multi-fin normally-off $Ga_2O_3$ vertical transistors with a breakdown voltage over 2.6 kV *Technical Digest—Int. Electron Devices Meeting, IEDM* vol 2019- Decem

Wang C, Zhou H, Zhang J, Mu W, Wei J, Jia Z, Zheng X, Luo X, Tao X and Hao Y 2022 Hysteresis-free and $\mu$s-switching of

D/E-modes $Ga_2O_3$ hetero-junction FETs with the BV²/Ron,sp of 0.74/0.28 GW/cm² *Appl. Phys. Lett.* **120** 112101

Wang C *et al* 2021 Demonstration of the p-NiOx/n-$Ga_2O_3$ heterojunction gate FETs and diodes with BV²/Ron,sp figures of merit of 0.39 GW/cm² and 1.38 GW/cm² *IEEE Electron Device Lett.* **42** 485–8

Liu Q *et al* 2024 1 kV β-$Ga_2O_3$ UMOSFET with quasi-inversion nitrogen-ion-implanted channel *Proc. Int. Symp. on Power Semiconductor Devices and ICs* pp 236–9

Zhou X, Ma Y, Xu G, Liu Q, Liu J, He Q, Zhao X and Long S 2022 Enhancement-mode β-$Ga_2O_3$ U-shaped gate trench vertical MOSFET realized by oxygen annealing *Appl. Phys. Lett.* **121** 223501

Ma Y *et al* 2023 702.3 A·cm²/10.4 mΩ·cm² β-$Ga_2O_3$ U-shape trench gate MOSFET with N-ion implantation *IEEE Electron Device Lett.* **44** 384–7

Wong M H, Murakami H, Kumagai Y and Higashiwaki M 2020 Enhancement-mode β-$Ga_2O_3$ current aperture vertical MOSFETs with N-ion-implanted blocker *IEEE Electron Device Lett.* **41** 296–9

Wong M H, Goto K, Murakami H, Kumagai Y and Higashiwaki M 2018 Current aperture vertical β-$Ga_2O_3$ MOSFETs fabricated by N- and Si-ion implantation doping *IEEE Electron Device Lett.* **40** 431–4

Zeng K, Soman R, Bian Z, Jeong S and Chowdhury S 2022 Vertical $Ga_2O_3$ MOSFET with magnesium diffused current blocking layer *IEEE Electron Device Lett.* **43** 1527–30

Ji D, Gupta C, Chan S H, Agarwal A, Li W, Keller S, Mishra U K and Chowdhury S 2018 Demonstrating >1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices *Technical Digest—Int. Electron Devices Meeting, IEDM* pp 9.4.1–4

Luo C, Yang C, Zhao Z, Xie X, Wei Y, Wei J, Shen J, Qiu J and Luo X 2024 Novel high-voltage GaN CAVET with high threshold voltage and low reverse conduction loss *Microelectron. J.* **148** 106195

Gake T, Kumagai Y and Oba F 2019 First-principles study of self-trapped holes and acceptor impurities in $Ga_2O_3$ polymorphs *Phys. Rev. Mater.* **3** 44603

Angeloni L A, Shan I-J, Leach J H and Schroeder W A 2024 Iron dopant energy levels in β-$Ga_2O_3$ *Appl. Phys. Lett.* **124** 252104

Ghadi H *et al* 2023 Identification and characterization of deep nitrogen acceptors in β-$Ga_2O_3$ using defect spectroscopies *APL Mater.* **11** 111110

Feng Z, Bhuiyan A F M, Kalarickal N K, Rajan S and Zhao H 2020 Mg acceptor doping in MOCVD (010) β-$Ga_2O_3$ *Appl. Phys. Lett.* **117** 222106

Jesenovec J, Weber M H, Pansegrau C, McCluskey M D, Lynn K G and McCloy J S 2021 Gallium vacancy formation in oxygen annealed β-$Ga_2O_3$ *J. Appl. Phys.* **129** 245701

Ingebrigtsen M E, Varley J B, Kuznetsov A Y, Svensson B G, Alfieri G, Mihaila A, Badstübner U and Vines L 2018 Iron and intrinsic deep level states in $Ga_2O_3$ *Appl. Phys. Lett.* **112** 042104

Wong M H, Lin C-H, Kuramata A, Yamakoshi S, Murakami H, Kumagai Y and Higashiwaki M 2018 Acceptor doping of β-$Ga_2O_3$ by Mg and N ion implantations *Appl. Phys. Lett.* **113** 102103

Kyrtsos A, Matsubara M and Bellotti E 2018 On the feasibility of p-type $Ga_2O_3$ *Appl. Phys. Lett.* **112** 032108

Peelaers H, Lyons J L, Varley J B and Van De Walle C G 2019 Deep acceptors and their diffusion in $Ga_2O_3$ *APL Mater.* **7** 022519

Lyons J L 2018 A survey of acceptor dopants for β-$Ga_2O_3$ *Semicond. Sci. Technol.* **33** 05LT02

Lyons J L, Wickramaratne D and Janotti A 2024 Dopants and defects in ultra-wide bandgap semiconductors *Curr. Opin. Solid State Mater. Sci.* **30** 101148

Zeng K, Bian Z, Sinha N and Chowdhury S 2024 Simultaneous drive-in of Mg and disassociation of Mg-H complex in $Ga_2O_3$ by oxygen annealing achieving remarkable current blocking *Appl. Phys. Lett.* **124** 212102

Oshima T, Kaminaga K, Mukai A, Sasaki K, Masui T, Kuramata A, Yamakoshi S, Fujita S and Ohtomo A 2013 Formation of semi-insulating layers on semiconducting β-$Ga_2O_3$ single crystals by thermal oxidation *Jpn. J. Appl. Phys.* **52** 0–5

Alema F, Itoh T, Brand W, Osinsky A and Speck J S 2023 Controllable nitrogen doping of MOCVD $Ga_2O_3$ using $NH_3$ *Appl. Phys. Lett.* **122** 252105

Mauze A, Zhang Y, Itoh T, Mates T E, Peelaers H, Van de Walle C G and Speck J S 2021 Mg doping and diffusion in (010) β-$Ga_2O_3$ films grown by plasma-assisted molecular beam epitaxy *J. Appl. Phys.* **130** 235301

Saha S, Meng L, Bhuiyan A F M, Sharma A, Saha C N, Zhao H and Singisetti U 2023 Electrical characteristics of *in situ* Mg-doped β-$Ga_2O_3$ current-blocking layer for vertical devices *Appl. Phys. Lett.* **123** 132105

Saha S, Amir W, Liu J, Meng L, Yu D, Zhao H and Singisetti U 2025 E-mode vertical β-$Ga_2O_3$ (010) U-trench MOSFETs with *in-situ* Mg-doped current blocking layers *IEEE Electron Device Lett.* **46** 725–8

Wong M H and Higashiwaki M 2020 Vertical β-$Ga_2O_3$ power transistors: a review *IEEE Trans. Electron Devices* **67** 3925

Hu Y *et al* 2025 High-temperature N ion implantation for performance-enhanced current-blocking layers in β-$Ga_2O_3$ *Appl. Phys. Lett.* **126** 112104

Xu X *et al* 2024 Nitrogen-doped $Ga_2O_3$ current blocking layer using MOCVD homoepitaxy for high-voltage and low-leakage $Ga_2O_3$ vertical device fabrication *Appl. Phys. Lett.* **125** 202107

He Q *et al* 2022 Selective high-resistance zones formed by oxygen annealing for β-$Ga_2O_3$ Schottky diode applications *IEEE Electron Device Lett.* **43** 1933–6

Liu Q, Zhou J, Zhou X, Wong M H, Yao H, Liu J, Zhang X, Xu G and Long S 2025 Improved blocking capability of

N-ion-implanted β-$Ga_2O_3$ U-shaped trench gate MOSFET by annealing in oxygen *Appl. Phys. Express* **18** 041003

Sharma R, Law M E, Ren F, Polyakov A Y and Pearton S J 2021 Diffusion of dopants and impurities in β-$Ga_2O_3$ *J. Vac. Sci. Technol. A* **39** 60801

Li M J *et al* 2024 High-performance β-$Ga_2O_3$ Schottky barrier diodes with Mg current blocking layer using spin-on-glass technique *Appl. Phys. Lett.* **125** 132101

Feng G, Suda J and Kimoto T 2012 Space-modulated junction termination extension for ultrahigh-voltage p-i-n diodes in 4 H-SiC *IEEE Trans. Electron Devices* **59** 414–8

Sung W and Baliga B J 2017 A comparative study 4500-V edge termination techniques for SiC devices *IEEE Trans. Electron Devices* **64** 1647–52

Malakoutian M *et al* 2025 Lossless phonon transition through GaN-diamond and Si-diamond interfaces *Adv. Electron. Mater.* **11** 2400146

Qin Y *et al* 2023 Thermal management and packaging of wide and ultra-wide bandgap power devices: a review and perspective *J. Appl. Phys.* **56** 093001